National Aviation University

Department of Electronics, Robotics, Monitoring and IoT Technologies

Course: "Fundamentals of Analog Electronics"

Experiment 6

"Differential Amplifier"

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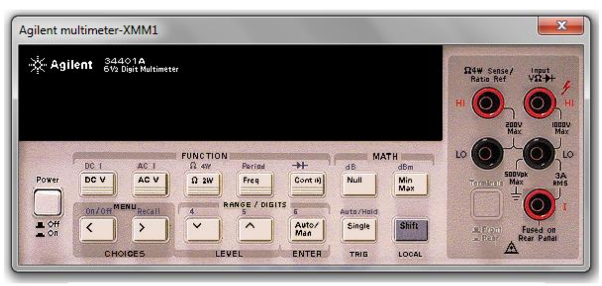
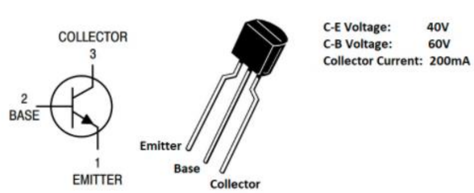
OBJECTIVES

1. To study the characteristics of differential amplifiers.
2. To measure the common-mode-rejection-ratio of the differential amplifier.
3. To simulate the differential amplifier using MULTISIM software.

EQUIPMENT

1. Digital multimeter: Agilent 34401A
2. Solderless breadboard: BB830T
3. Oscilloscope: Agilent 54622D
4. Sinusoidal generator: 1 × 10 kHz
5. Power Supplies: 2 × 15 V
6. Transistors: 2 × 2N3904
7. Resistors: 2 × 4.7 kΩ, 1 × 22 kΩ





Theory

The input stage of most operational amplifiers is a *differential amplifier*, shown in its simplest form in Fig. 1.

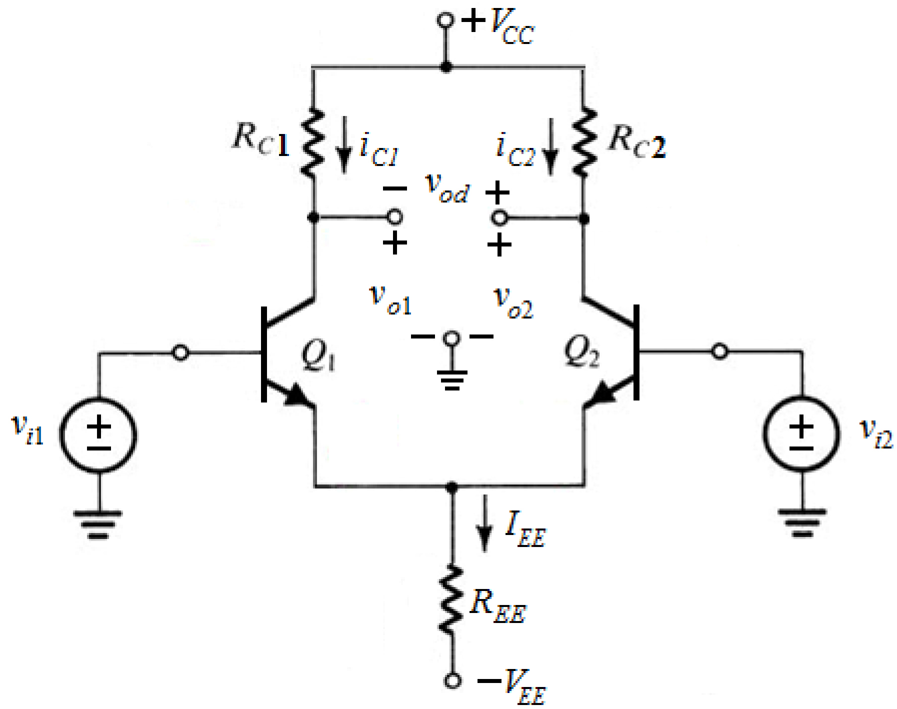


Fig. 1 Differential BJT amplifier

The function of a differential amplifier is to amplify the difference between two signals. It operates from *dc* to several hundred MHz. The differential amplifier consists of two emitter-coupled common-emitter amplifiers with two inputs, v_{i1} and v_{i2}, and three outputs, v_{o1}, v_{o2}, and v_{od}. The third output is the difference between $v_{o1}$and v_{o2}.

Ideally R_{EE} should be infinite. In this case input resistance will also be infinite and the circuit will operate as an ideal differential amplifier. The characteristics of the ideal differential amplifier are as follows:

1) for identical inputs the outputs are zero;

2) for different inputs the output is proportional to the difference between the inputs.

Because Q_1 and Q_2 must have dc bias, the size of R_{EE} is limited. If R_{EE} is increased, the negative supply voltage, $-V_{EE}$, must also be increased in order to maintain the same dc bias current for two transistors.

The differential amplifier is intended to respond only to the difference between the two input ac voltages, v_{i1} and v_{i2}. However, in a practical differential amplifier the output depends to some degree on the sum of these inputs. For example, if both inputs are equal, the output voltage should be zero but in a practical amplifier it is not. When the circuit responds to the difference, we say it is in the differential mode. If the two inputs are equal, the circuit is in its common mode.

Any two input voltages can be expressed through a common and a differential part. We define two new input voltages as follows:

$$v_{id} = v_{i1} - v_{i2}$$

$$v_{ic} = \frac{v_{i1} + v_{i2}}{2}$$

The voltage v_{ic}, the common-mode input voltage, is the average of the two input voltages.
The original input voltages can be expressed in terms of these two new quantities as follows:

$$v_{i1} = \frac{v_{id} + 2v_{ic}}{2} \qquad (1)$$

$$v_{i2} = \frac{2v_{ic} - v_{id}}{2}$$

Assuming $v_{i2} = -v_{i1}$, we obtain the differential mode with

$$v_{ic} = 0, \;\; v_{i1} = \frac{v_{id}}{2}, \text{ and } v_{i2} = -\frac{v_{id}}{2}$$

A hybrid-π model shown in Fig. 2, with $r_{bb'}$, $r_{b'c}$ and r_o neglected, is used to construct the small-signal model with a differential input voltage.

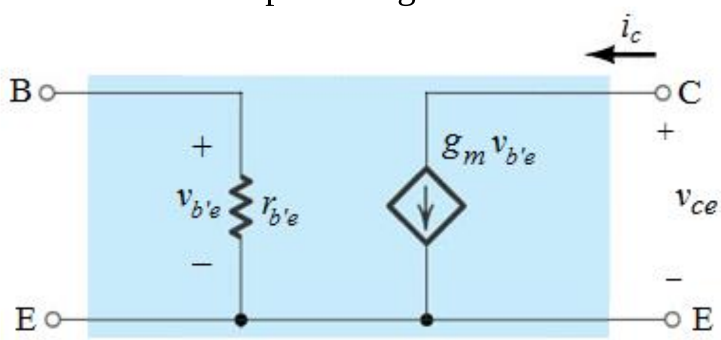


Fig. 2. Simplified hybrid-π model of a BJT

The differential mode small-signal equivalent circuit is shown in Fig. 3.

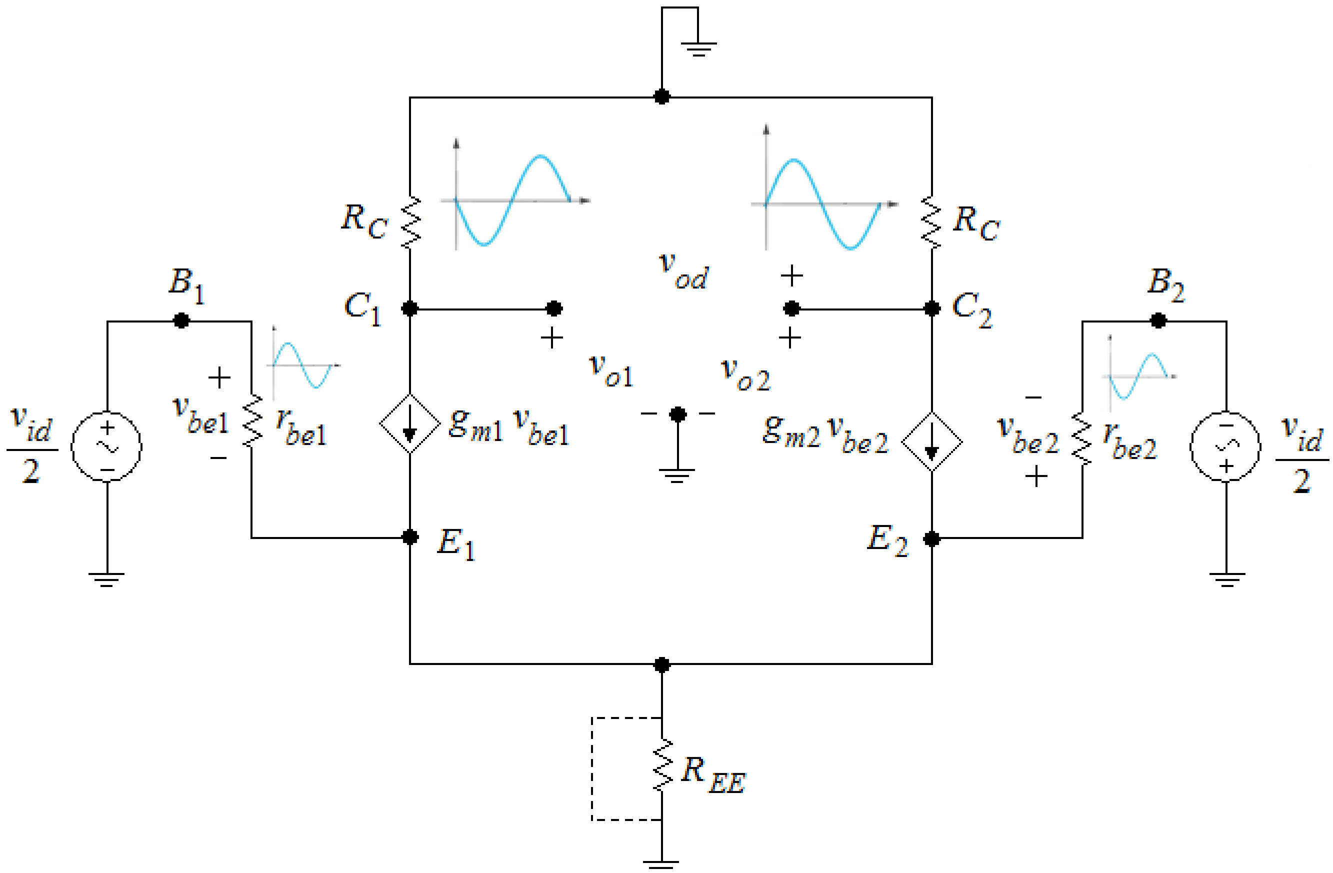


Fig. 3. Differential mode small-signal equivalent circuit

Because $I_{C1} = I_{C2}$, then

$$g_{m1} = g_{m2} = \frac{1}{h_{ib}} = \frac{I_{C1}}{V_T} = \frac{I_{EE}}{2V_T}$$

Note that when the current i_{C1} is increasing the current i_{C2} is decreasing at the same rate and amplitude. This is true because the input to Q_2 is equal to that of Q_1 but 180° out of phase. Thus the voltage change across R_{EE} is zero and it can be replaced by a short circuit in the *ac* equivalent circuit. The voltages v_{o1} and v_{o2} will be of equal amplitude and opposite phase.

The differential gain is

$$A_d = \frac{v_{o1}}{v_{i1} - v_{i2}} = \frac{v_{o1}}{\frac{v_{id}}{2} - \left(-\frac{v_{id}}{2}\right)} = \frac{v_{o1}}{v_{id}} \qquad (2)$$

The output voltage is given by

$$v_{o1} = -g_m v_{be1} R_C \tag{3}$$

and the input voltage is

$$\frac{v_{id}}{2} = v_{be1} \text{ or } v_{id} = 2v_{be1} \tag{4}$$

Substituting (3) and (4) into (2), gives

$$A_d = \frac{-g_m v_{be1} R_C}{2v_{be1}} = -\frac{g_m R_C}{2}$$

Since $g_m = \frac{1}{h_{ib}}$, then

$$A_d = -\frac{R_C}{2h_{ib}}$$

The differential mode gain A_d is a single-ended output because it is taken between one collector to ground. If the output is taken between v_{o1} and v_{o2}, the differential mode gain is called a double-ended output and is

$$A_d' = \frac{v_{od}}{v_{id}} = \frac{v_{o1} - v_{o2}}{v_{id}} = \frac{v_{o1} - (-v_{o1})}{v_{id}} = \frac{2v_{o1}}{v_{id}} = -\frac{R_C}{h_{ib}}$$

A common mode equivalent circuit is shown in Fig. 4. The voltage at each collector will be in phase in contrast to the out-of-phase collector voltage relationship for a differential input voltage. Each collector voltage will be called the common mode output voltage, v_{oc}.

If we divide the resistor R_{EE} into two parallel resistors that each has double the original resistance, we can find the output by analyzing only half the circuit as shown in Fig. 5.

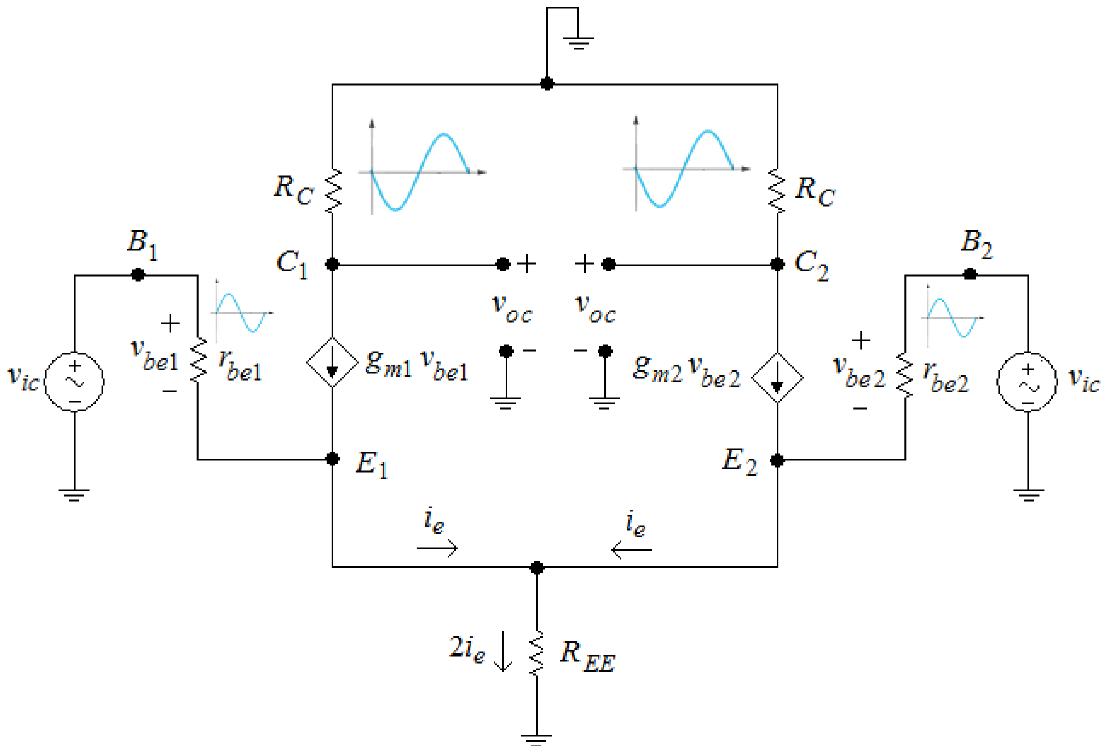


Fig. 4. Small-signal model with a common-mode input signal

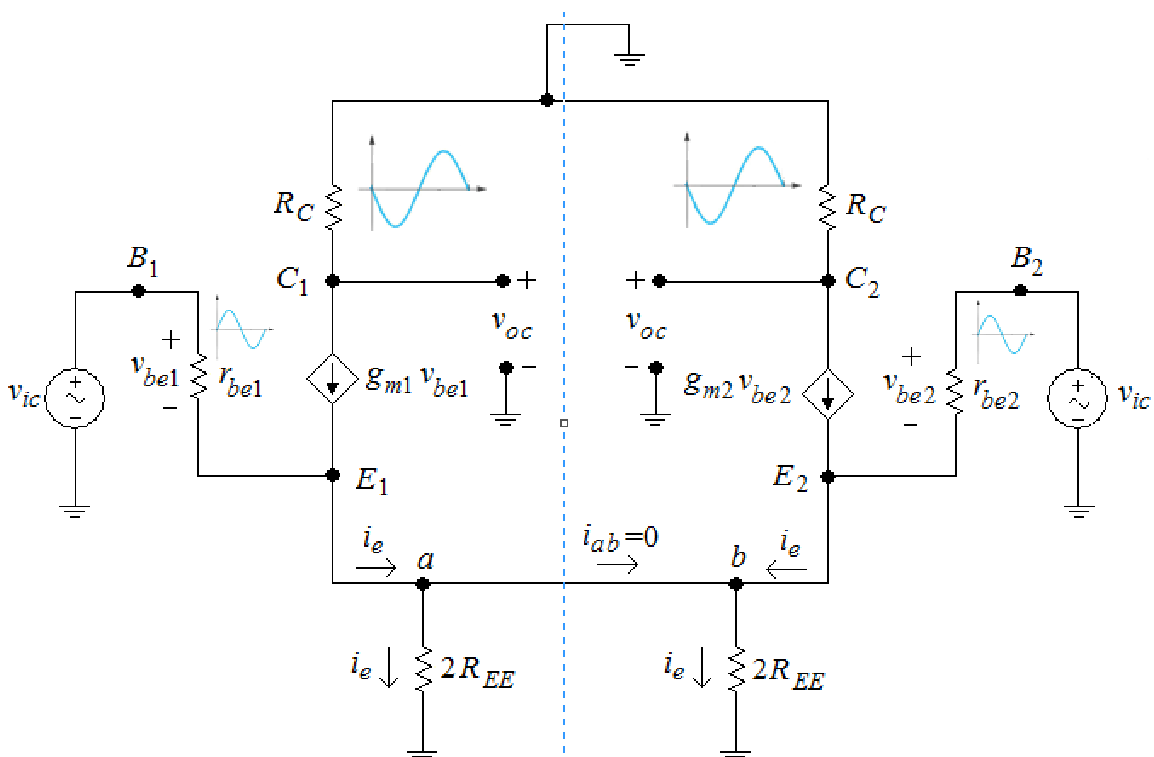


Fig. 5. Decomposition of R_{EE} for the common-mode small-signal model

Since the transistors are identical and the common-mode input voltages are equal and in phase, the voltages across the $2R_{EE}$ resistors are the same. Thus, the current i_{ab} is zero, and we need only to look at one side of the circuit, which is separately shown in Fig. 3.

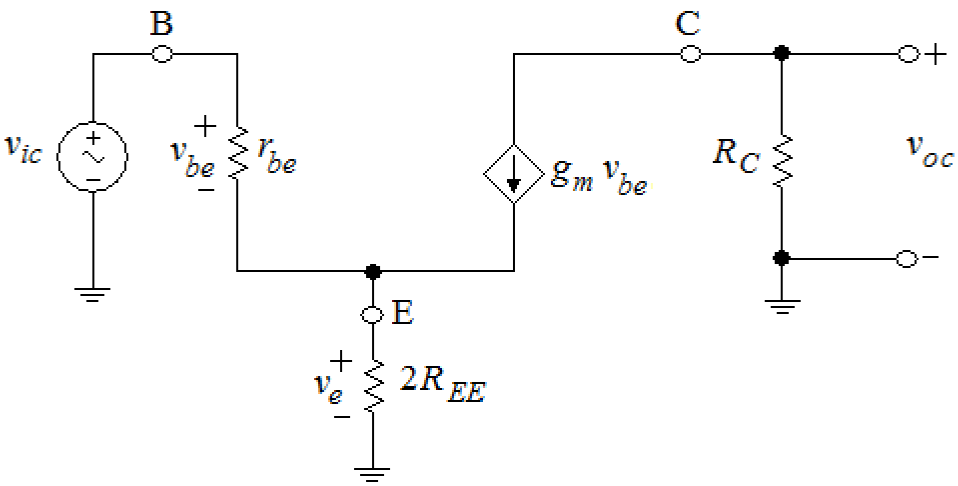


Fig. 6. Half-circuit model

The common-mode gain is defined as

$$A_c = \frac{v_{oc}}{v_{ic}} \tag{5}$$

The output voltage, v_{oc}, is determined as follows

$$\frac{v_{oc}}{R_C} + g_m v_{be} = 0$$

and finally

$$v_{oc} = -g_m v_{be} R_C \tag{6}$$

For the input loop we have

$$v_{ic} = v_{be} + v_e = v_{be} + 2R_{EE} g_m v_{be} = v_{be}(1 + 2g_m R_{EE}) \tag{7}$$

Substituting v_{oc} and v_{ic} from Eq. (6) and Eq. (7) into Eq. (5), gives

$$A_c = -\frac{g_m R_C}{1 + 2g_m R_{EE}} \tag{8}$$

Assuming $2g_m R_{EE} >> 1$, Eq. (8) reduces to

$$A_C \cong -\frac{R_C}{2R_{EE}} \tag{9}$$

For example, if R_C = 4.7 kΩ and R_{EE} = 22 kΩ, then

$$A_c = -\frac{4.7}{2\times 22} = -0.107$$

It is desirable for the differential mode gain to be much larger than the common mode gain so that the amplifier will react only to the difference between the input voltages. The common-mode rejection ratio (CMRR) is defined as the ratio of A_d to A_c

$$\mathrm{CMRR} = \frac{A_d}{A_C} = \frac{-g_m R_C/2}{-g_m R_C/(1+2g_m R_{EE})} = 0.5 + g_m R_{EE} \approx g_m R_{EE} \tag{10}$$

or in dB

$$(\mathrm{CMRR})_{dB} = 20\log\frac{A_d}{A_C} = 20\log(g_m R_{EE}) \tag{11}$$

Since $g_m = 1/h_{ib}$, then

$$\mathrm{CMRR} = \frac{R_{EE}}{h_{ib}} = \frac{I_{EE}R_{EE}}{2V_T} \tag{12}$$

Example 1. Compute the CMRR for the amplifier if I_{EE}=0.65mA, R_{EE}=22kΩ and V_T = 26mV.

Solution.

$$\mathrm{CMRR} = \frac{I_{EE}R_{EE}}{2V_T} = \frac{0.65\times 22\times 10^3}{2\times 26} = 275$$

or

$$(\mathrm{CMRR})_{\mathrm{dB}} = 20\log 275 = 48.9\mathrm{dB}$$

The CMRR can be improved by increasing I_{EE} or R_{EE}. However, this design alternative might not be acceptable because R_{EE} might be too large for monolithic IC fabrication, or the power supply voltage, V_{EE}, might become too large.

PROCEDURE

1. Construct the BJT differential amplifier circuit (see Fig. 7) operating in differential mode.
2. Turn on +15 V and -15 V power suppies.
3. Adjust the FREQUENCY control of signal generator so the input is 10 kHz sinusoidal waveform with 20 mV peak amplitude (14.2 mV rms).
4. Measure the voltage amplitude of the output voltage Vod. Record the voltage measurement.
5. Measure the voltage amplitude going from the generator into the amplifier Vid. Record the voltage measurement.
6. Use the formula $A_d = V_{od}/V_{id}$ to calculate the voltage gain. Record the voltage gain calculation.
7. Construct the BJT differential amplifier circuit (see Fig. 8) operating in common mode.
8. Adjust the FREQUENCY control of signal generator so the common input is 10 kHz sinusoidal waveform with 20 mV peak amplitude (14.2 mV rms).
9. Measure the common output voltage amplitude V_{oc}. Record the voltage measurement.
10. Use the formula $A_C = V_{oc}/V_{ic}$ to calculate the common mode gain. Record the common mode gain calculation.
11. Calculate the common mode rejection ratio by formula. Go to step 12 on page 11.

$$\left(\text{CMRR}\right)_{dB} = 20\log\frac{A_d}{A_C}.$$

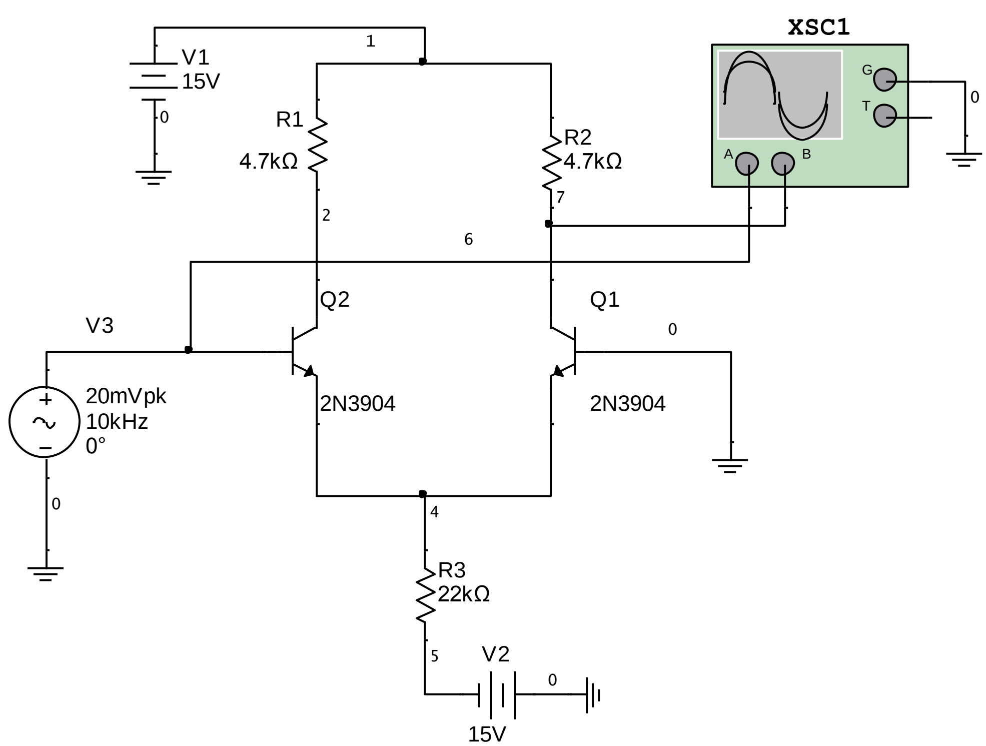


Fig. 7. Experimental BJT differential amplifier circuit diagram operating in differential mode.

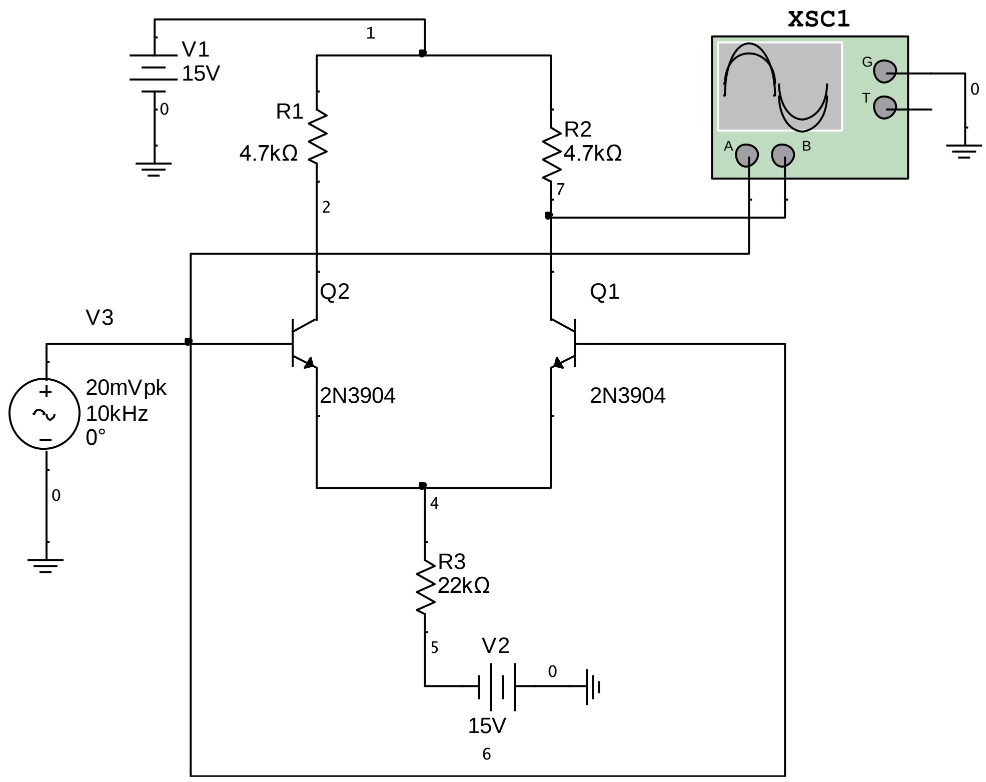


Fig. 8. Experimental BJT differential amplifier circuit diagram operating in common mode.

12. Construct the BJT differential amplifier circuit (see Fig. 9) with a simple current mirror operating in differential mode.
13. Measure the voltage amplitude of the output voltage V_{od}. Record the voltage measurement.
14. Use the formula $A_d = V_{od}/V_{id}$ to calculate the voltage gain. Record the voltage gain calculation.
15. Construct the BJT differential amplifier circuit (see Fig. 10) with a simple current mirror operating in common mode.
16. .Measure the voltage amplitude of the output voltage V_{oc}. Record the voltage measurement.
17. Use the formula $A_C = V_{oc}/V_{ic}$ to calculate the common mode gain. Record the common mode gain calculation.
18. Calculate the common mode rejection ratio by formula.

$$(\mathrm{CMRR})_{dB} = 20\log\frac{A_d}{A_C}.$$

19. Make conclusions on the values of CMRR calculated for circuits 7, 8 and 9, 10.

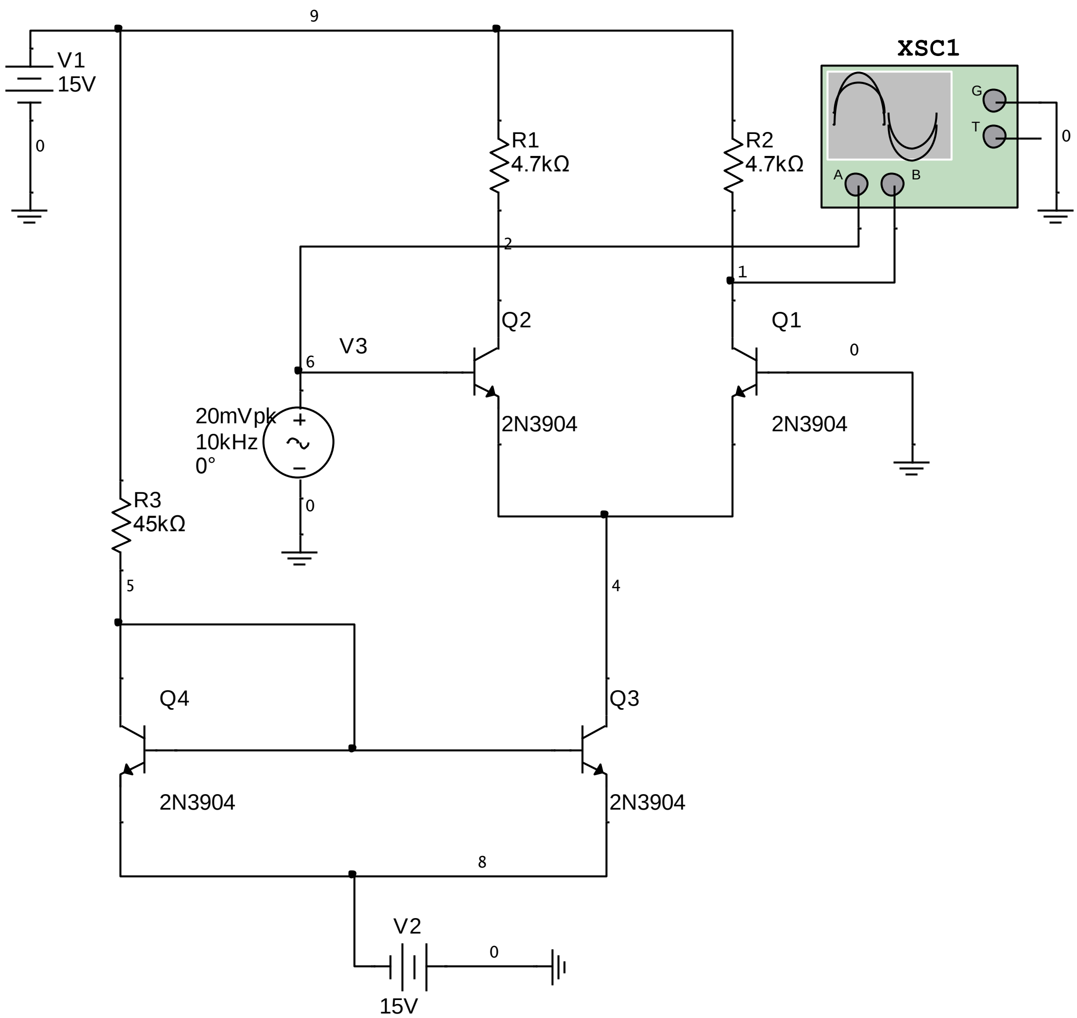


Fig. 9. Experimental BJT differential amplifier with a simple current mirror circuit diagram operating in differential mode.

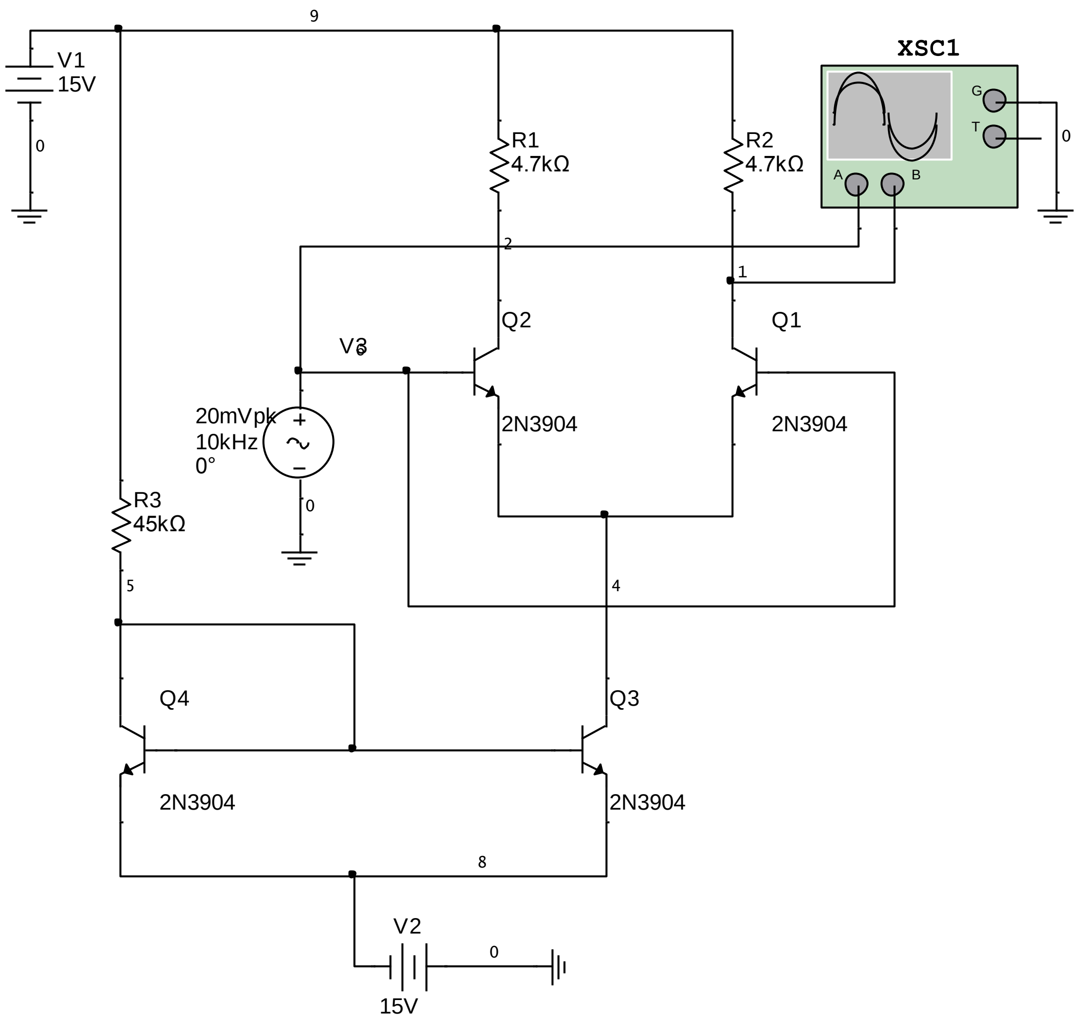


Fig. 10. Experimental BJT differential amplifier with a simple current mirror circuit diagram operating in common mode.

Reference

1. A.S. Sedra and K.S. Smith, "Microelectronic circuits", 5th ed., New York: Oxford University Press, 2004, 1283 p.